Quantitative Extraction and Compensation of Excess Inductance : Case Study of a Digital Attenuator Chip

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Abstract — **The excess inductance of the conductor connecting the ground pins of the MMIC and the ground plane is extracted from a simplified procedure of measurement and optimization. The method is applied to a digital attenuator chip with a positive bias circuit. The addition of bypass capacitors with the value compensating the extracted excess inductance of the conductor clearly improves the performance of the chip.**

I. INTRODUCTION

Most commercial GaAs MESFET MMIC chips use negative biases since the metal gate should be reverse-biased for the channel control. When those chips are surface-mounted on printed circuit boards (PCBs), they are grounded by directly connecting ground pins to the ground plane through via holes. Then the return current path from the ground pin to the ground plane becomes the shortest one, which is normally required by general RF design. On the other hand, many practical RF systems operate with only positive biases. In such cases, extra biasing circuits are required and the ground pins are separated from the ground plane by DC blocking capacitors. Therefore, in an AC state, the return current path becomes longer. The long ground path provides excess inductance components that influence the operation of the chip.

In this paper, a methodology of extracting excess inductance of long ground paths is presented. The procedure of extracting is as follows: (1) fabricating and characterizing a simplified passive network (test board) which simulates the function of the chip; (2) constructing an equivalent circuit of the test board including the excess inductance of the ground path; (3) extracting the excess inductance by utilizing the optimization procedure of the ADS [1] and the measured results. The model chip used in this work is a GaAs MESFET 15.5 dB digital attenuator with the attenuation step of 0.5 dB [2]. The chip is normally negative-biased and the ground path problem occurs when it is connected with the bias conversion circuit. A scheme of 14 dB π-attenuator is used with the board layout whose grounding geometry is the same as that of the chip. The value of the decoupling capacitance is determined by the extracted inductance and the successful positive bias operation is demonstrated.

The effect of parasitic components can be analyzed by the partial element equivalent circuit (PEEC) in the frequency domain [4]. Such a multi-conductor approach is generally accurate when it is supported by an accurate parameter extraction procedure such as 3D field simulation [5] or measurement/optimization [1]. Our technique is a simple form of the PEEC with a parameter extraction by measurement/optimization. Furthermore, our model case shows that the modeling of the whole ground plane is not necessary and the modeling of only the critical portion could be enough.

II. EXPERIMENTS AND EXTRACTION OF EXCESS INDUCTANCE

Figure 1 (a) shows the schematic of the bias circuit connected to the ground pins of the chip and Fig. 1 (b) shows the actual board layout. The inclusion of the bias circuit requires a conductor with a finite length between the ground pins and the DC blocking capacitors (denoted by the dotted square). Figure 2 shows the measured attenuation results of the actual test board in the frequency range from 1.74 to 1.88 GHz (PCS band in Korea). The attenuation steps are not evenly spaced and some of them are even overlapped with one another.

A 14 dB π-attenuator modeling the grounding of the chip is fabricated and measured. Figure 3 (a) shows the test board for modeling and Fig. 3 (b) shows the equivalent circuit. The π-attenuator is composed of 3 resistors and the microstrip line scheme on the FR-4 substrate is used. The measured DC resistances of the used resistors are 75.5 and 116.6 Ω, respectively. The equivalent circuit of the transition between the SMA connector and the microstrip line is explained elsewhere [6, 7]. The excess inductance originated from the conductor

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between the 75.5 Ω resistors and the via holes is represented by L_{eff}. Figure 4 shows the measured attenuation (S_{21}, solid lines) and the calculated attenuation (dotted lines) obtained from π-attenuators with different length of the conductor (D = 1 ~ 4 mm). The attenuation error becomes larger as the value of D increases and the maximum difference reaches 1.2 dB at 2.4 GHz. The calculated attenuation is obtained by optimizing L_{eff} with respect to the measured data. The dashed line shows the result when $L_{eff} = 0$. The average error ranges from 0.3 dB (when D = 1 mm) to 0.7 dB (when D = 4 mm).

Figure 5 shows the extracted L_{eff} versus D. Almost linear dependence on D is identified. The extrapolation to the D = 0 point gives the L_{eff} value of 0.45 nH. This value is originated from the self-inductance of the ground plane [8].

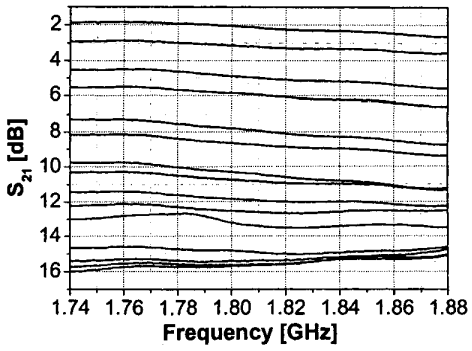
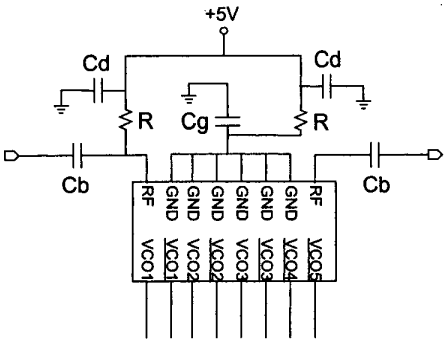


Fig. 2 The measured results of a 15.5dB digital attenuator with the long return path.

(a)



(b)

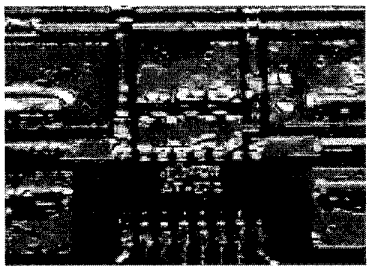
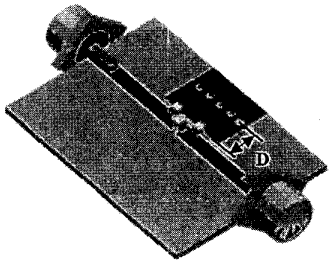


Fig. 1 (a) The bias conversion circuit [3] and (b) the actual attenuator board with the conversion circuit.

(a)



(b)

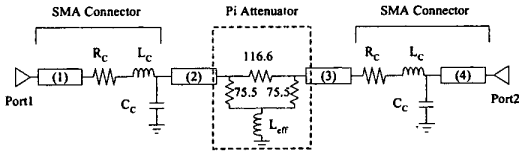


Fig. 3 (a) Test board and (b) the schematic diagram of the 14 dB fixed π-attenuator

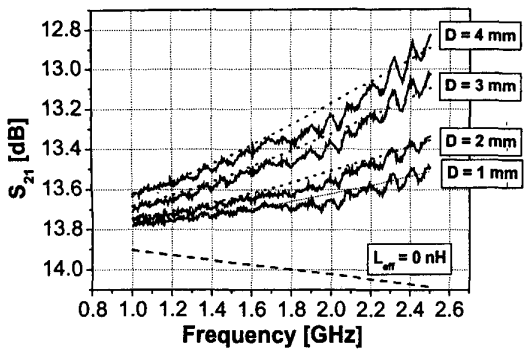


Fig. 4 The measured (solid lines) and the optimized (dotted lines) data of the 14 dB fixed π-attenuator with various values of D.

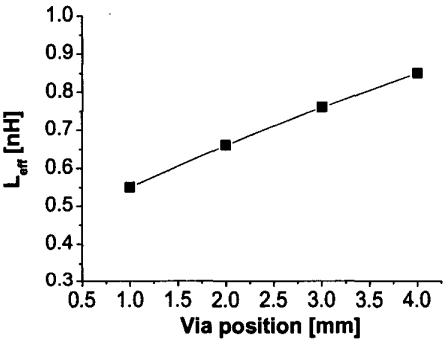


Fig. 5 The dependence of effective inductance (L_{eff}) on D

III. APPLICATION TO THE DIGITAL ATTEUNATOR

In Fig. 2 (a), the distance between the ground pins to the via holes is 4 mm. From the result of π-attenator, the value of L_{eff} is 0.85 nH when D = 4 mm and this gives the reactance of + j10 Ω at 1.8 GHz. For the cancellation of this excess reactance, two commercial capacitors with the capacitance value of 4.7 pF (total capacitance of 9.4 pF corresponding to the reactance of about – j10 Ω) are added between the problematic conductor and the ground. Figure 6 (a) shows the board with the compensation by the bypass capacitors. The black squares denote the position of the capacitors. Figure 6 (b) shows the measured attenuation. Almost ideal 1 dB steps can be identified.

Figure 7 (a) ~ (d) show the effect of the added bypass capacitors more clearly. The total value of the bypass capacitors increases from 2 pF (Fig. 7 (a)) to 14 pF (Fig. 7 (d)). The uniformity and the accuracy of the attenuation steps in the given frequency interval become better as the capacitance of the bypass capacitor increases. These results verify that two capacitors with the capacitance of 4.7pF can remove the excess inductance effectively in the previous work.

(a)

(b)

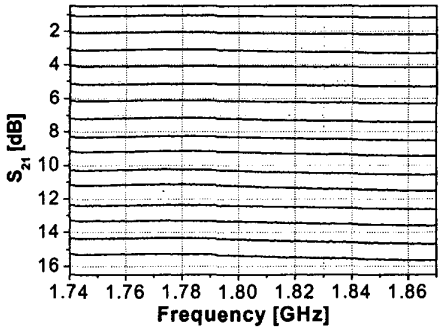


Fig.6 (a) Test board of the 15.5 dB digital attenuator with the bypass capacitors and (b) the measured results.

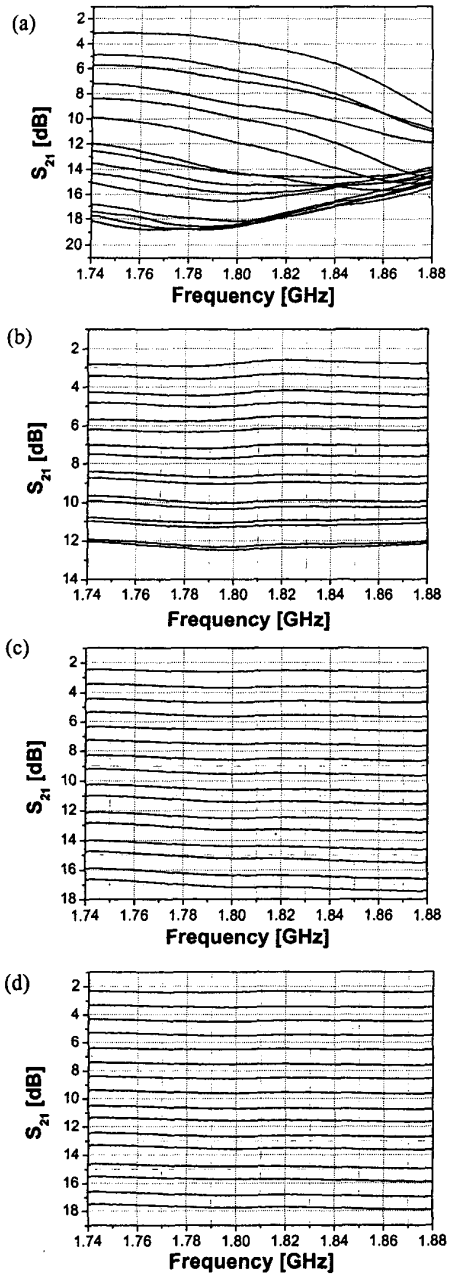


Fig. 7 The measured results of the digital attenuators with various values of the bypass capacitors : (a) 1 pF, (b) 3 pF, (c) 5 pF, (d) 7 pF.

IV. CONCLUSIONS

The method of quantitative extraction and compensation of the excess inductance is presented in the case of the digital attenuator chip. The extraction of the excess inductance is performed (1) by the fabrication and characterization of the simplified passive network simulating the function of the attenuator chip, and (2) by utilizing the optimization procedure of the equivalent circuit parameters. It is demonstrated experimentally that the addition of bypass capacitors compensates the effect of inductive component of the long conductor (return path).

ACKNOWLEDGEMENT

This work is supported by the Brain Korea 21 project.

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